Resonant Switched Capacitor Converters for High-Density Power Delivery

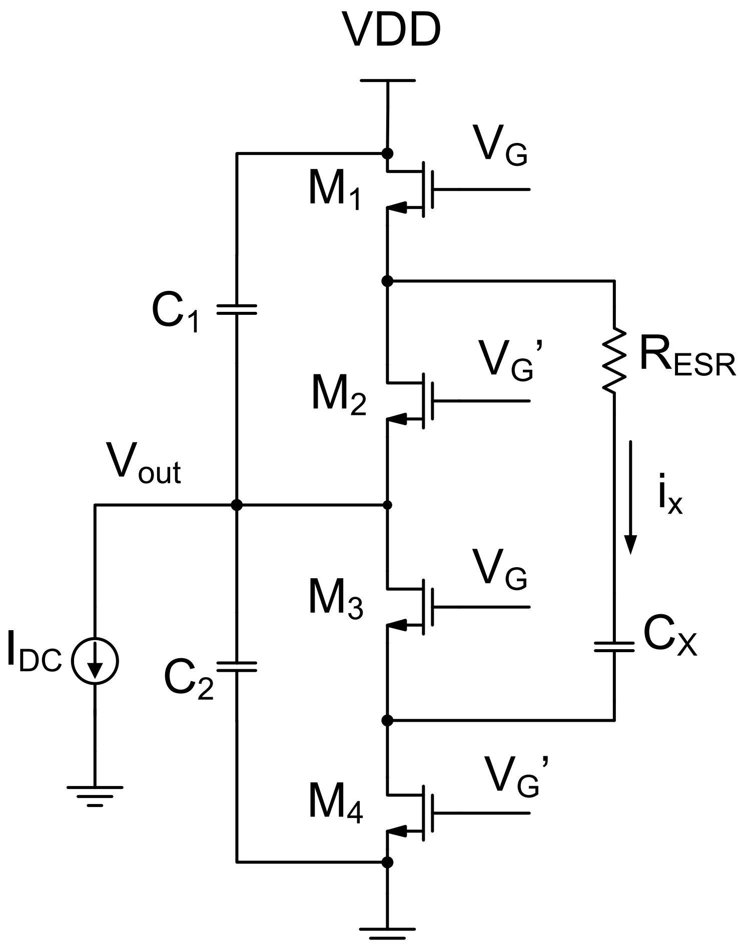
Jason T. Stauth
Assistant Professor
Dartmouth College
jason.stauth@dartmouth.edu

Motivation

- Applications that demand: **high density + efficiency**

Application		**Trends**
Mobile Devices & Communication		Pressure on battery life, size, cost, # converters
Performance Computing		# cores, density, integration, parasitics
Renewable Energy, Automotive	 	Extreme cost pressure, reliability

Switched Capacitor Converters



- Growing interest as candidate for monolithic DC-DC

+ High energy density of Si-integrated capacitors (compared to inductors)

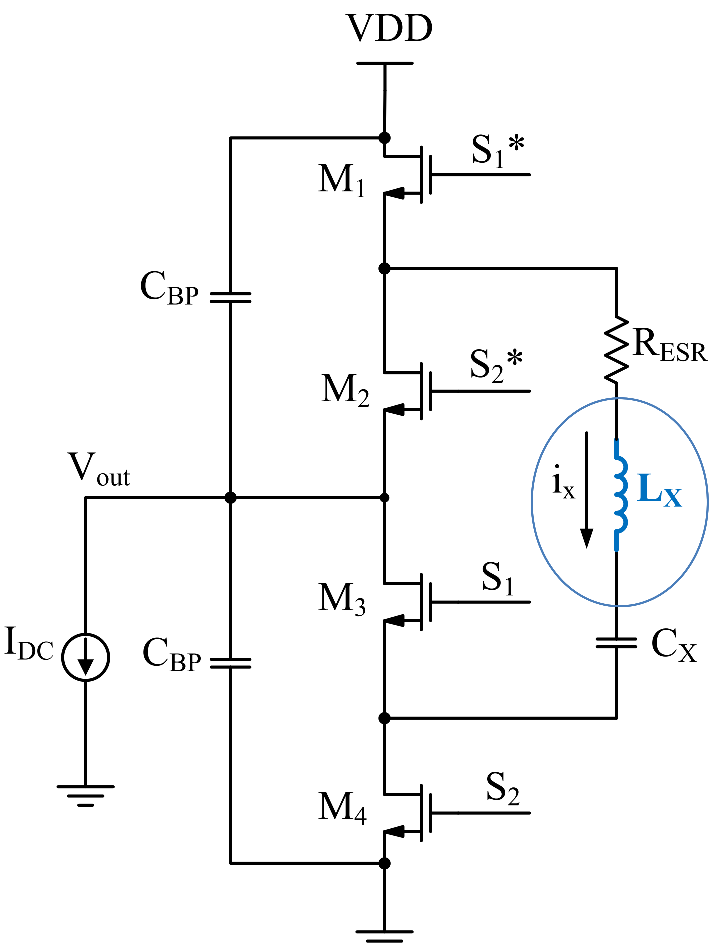
+ **Higher device utilization FOM*** compared to traditional DC-DC converter topologies

+ Deep-trench capacitors & scalable CMOS processes

+ No Inductors

***M. D. Seeman et. al, *IEEE TPEL*, 2008**

Resonant Switched Capacitor Converters



Kesarwani et. al. , *ISSCC, 2014*

Similarities to SC Converters:

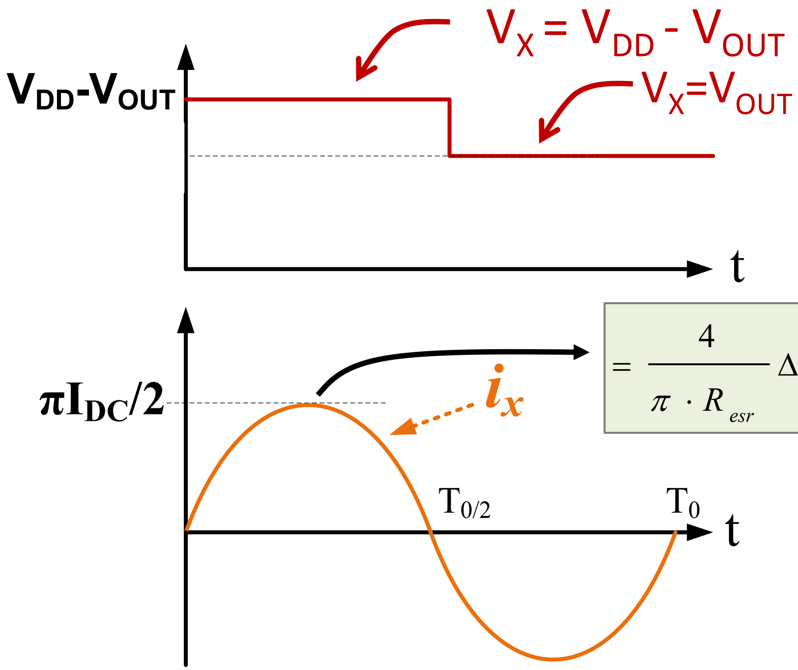
- Similar architectures (Ladder, Dickson, Series-Parallel, etc)
- Favorable device utilization FOMs
- Leverage high-density capacitors

Potential Advantages:

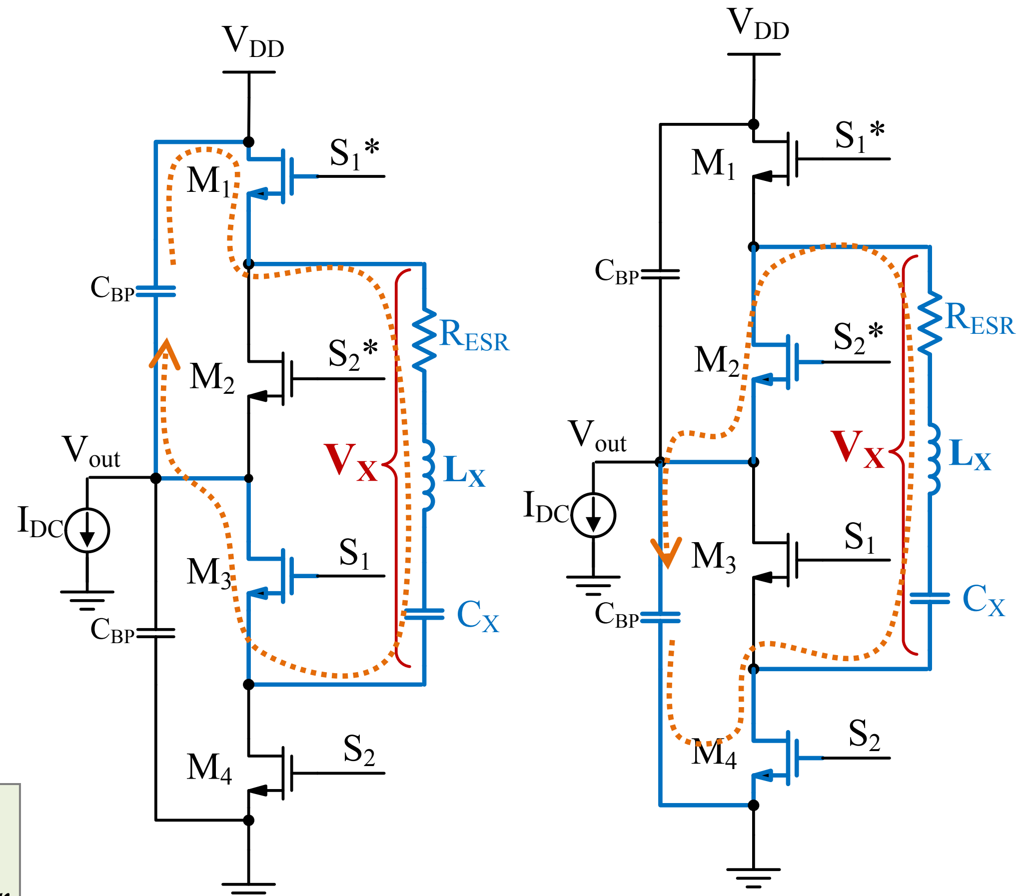
- Small magnetic component (few nH) resonates out reactive impedance (better capacitance utilization + soft switching)
- Improved trade-offs between switching (+bottom plate) loss and conduction loss

Resonant Operation

Nominal 2:1 Converter



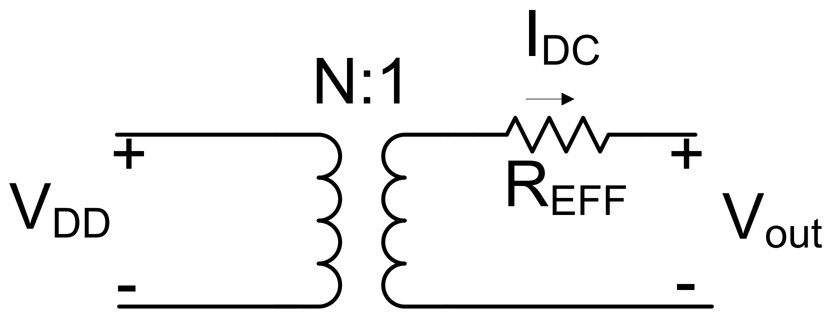
$$= \frac{4}{\pi \cdot R_{esr}} \Delta V$$



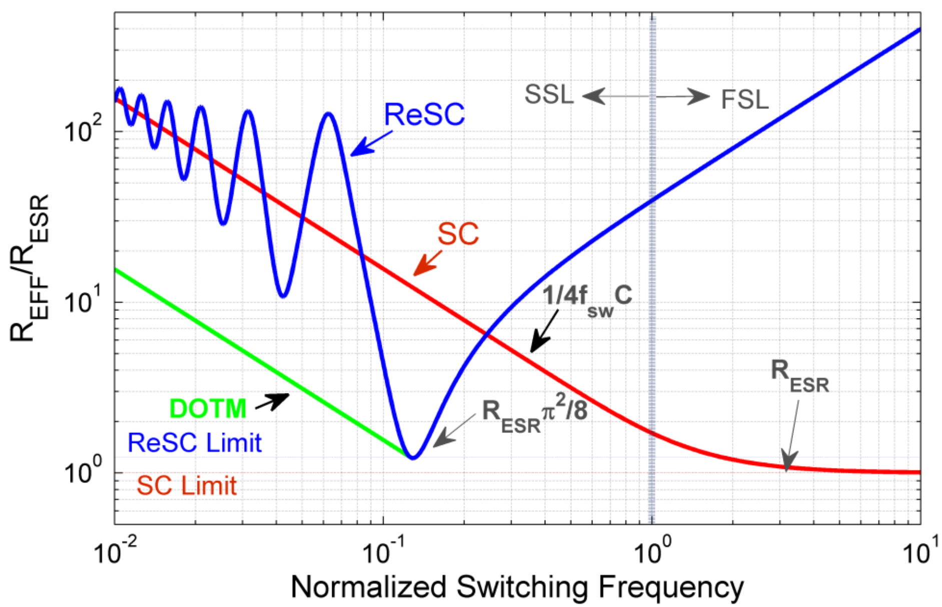
Averaged Steady State Conditions:

$$R_{EFF} \approx \frac{\pi^2}{8} R_{esr}$$

Effective Resistance



Transformer Model



- R_{EFF} models the effective output impedance of the converter
- SC in FSL: energy transfer is limited by ESR
- ReSC: Comparable minimum R_{EFF}, but at lower frequency
- Sub-harmonic operation for light load
- Burst mode even better[1]

[1] Kesarwani & Stauth, [*ISSCC '14*]

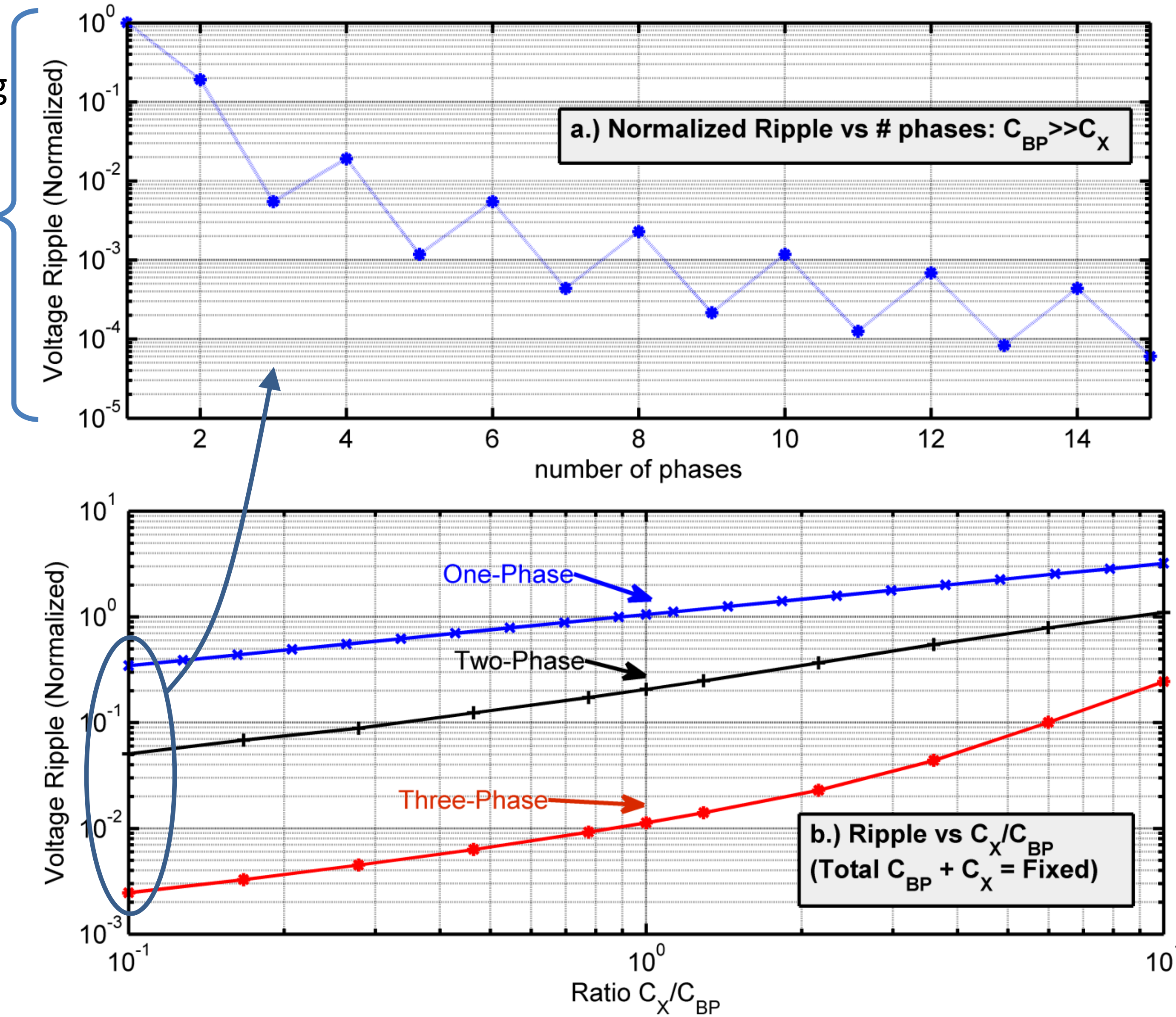
"Dynamic Off-Time Modulation (DOTM)"

Interleaving in ReSC

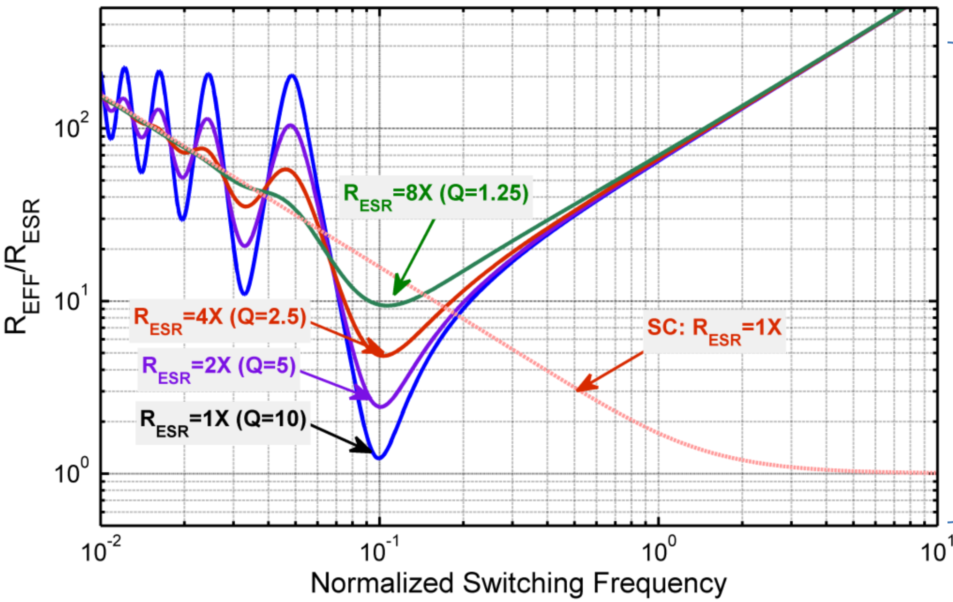
- Odd-order interleaving is better
- 3-phase → multiple order of magnitude improvement compared to 1-phase

When total die area is constrained:

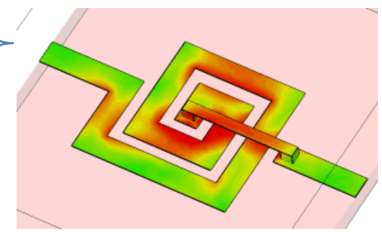
- More bypass → lower ripple
- With interleaving can allocate more to CX → Major improvements

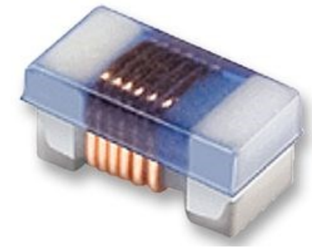


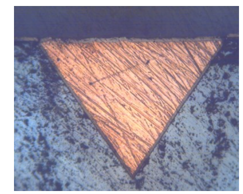
Limitations and Disadvantages



Need Inductive Component
→ Potential increase in ESR



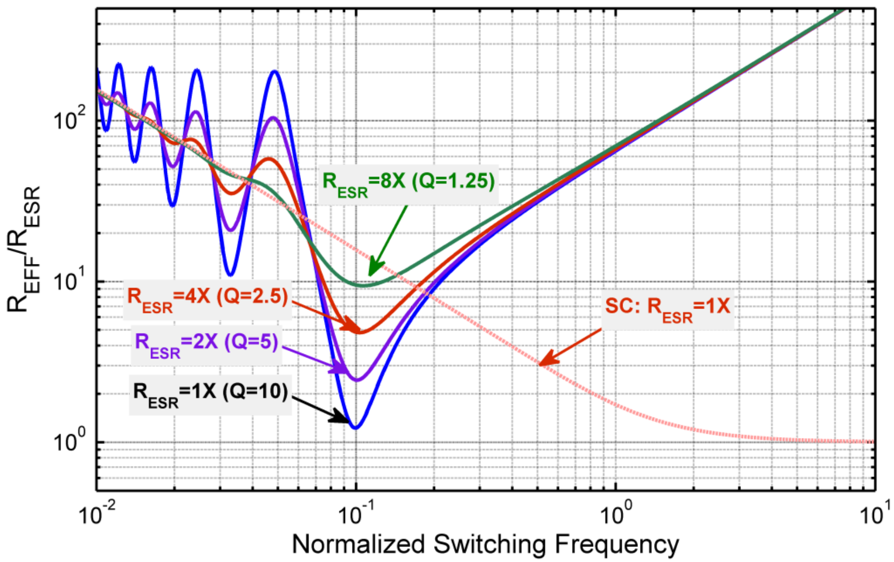




Summary (limitations)

- Need magnetic component(s)
  (Design goal is low ESR in resonant loop)
- Need 'some' explicit bypass capacitance
- Practical limitations on interleaving
  (Inductor scaling considerations)

Limitations and Disadvantages



Nonetheless:

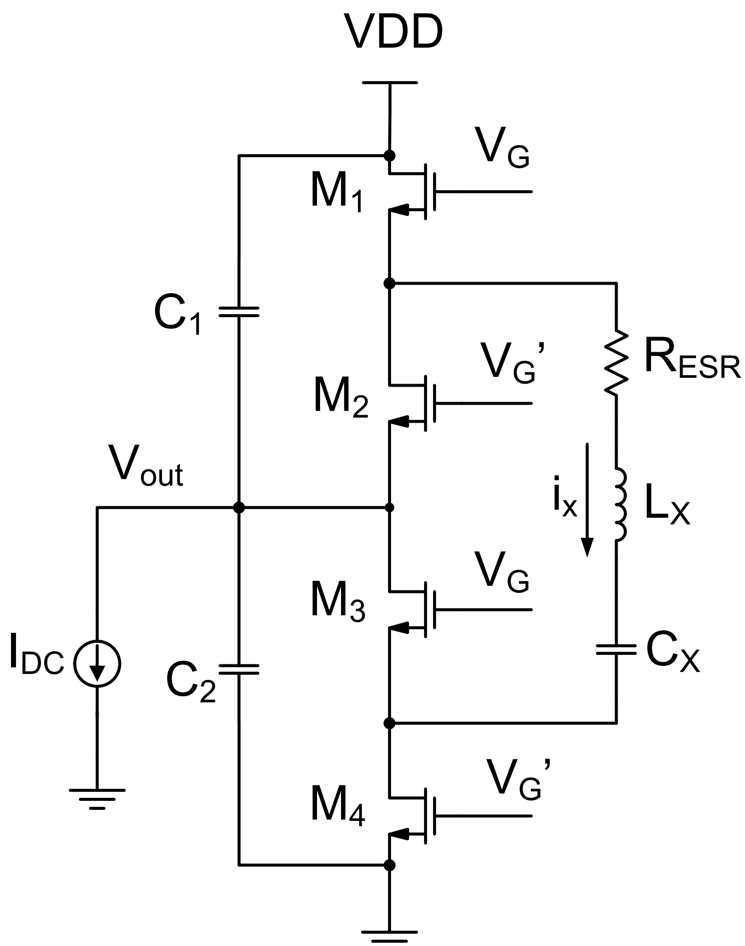
- Favorable operation with *very small* inductors
- Lower f_{SW} → can **reduce** ESR in capacitors and interconnect (parasitics we often don't talk about!)

Full analysis, optimization, and comparison is complicated:

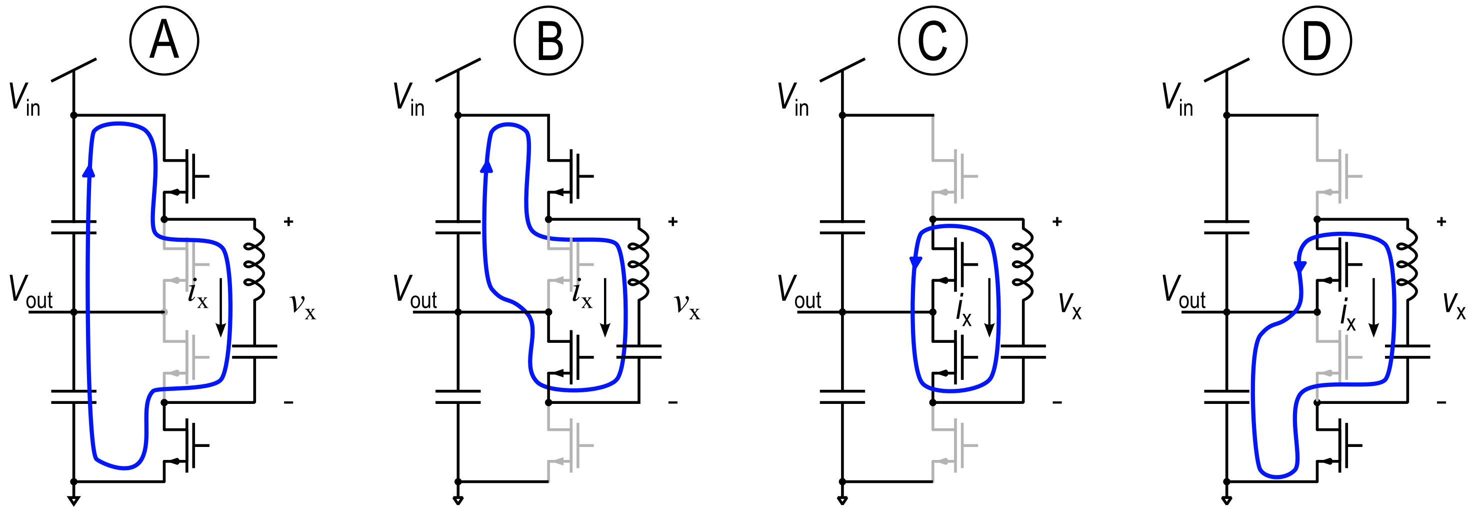
*Kesarwani & Stauth, COMPEL 2013

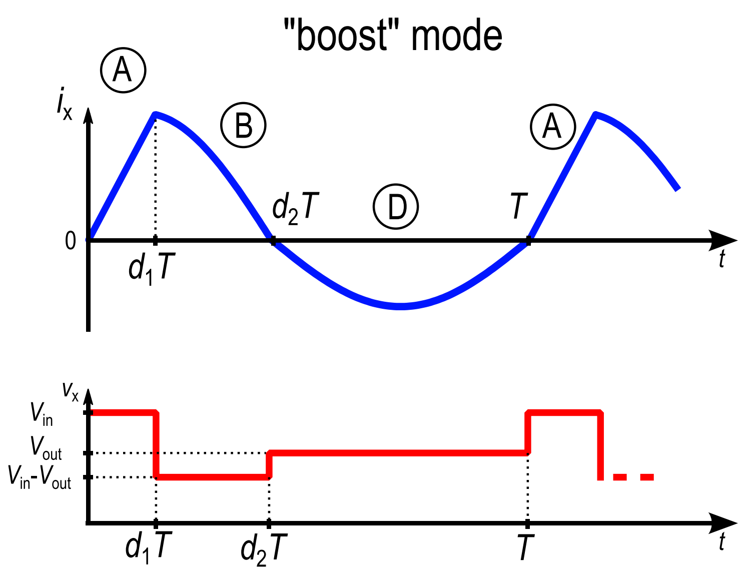
*Kesarwani & Stauth, TPEL 2015 (coming)

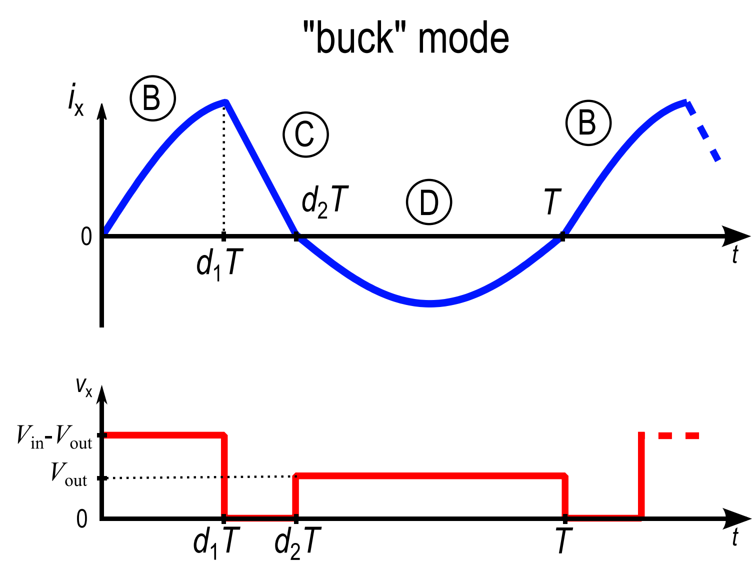
Major Opportunity & Potential Advantage: Efficient & Granular Variable Conversion Ratios



Example –Step Up/Down





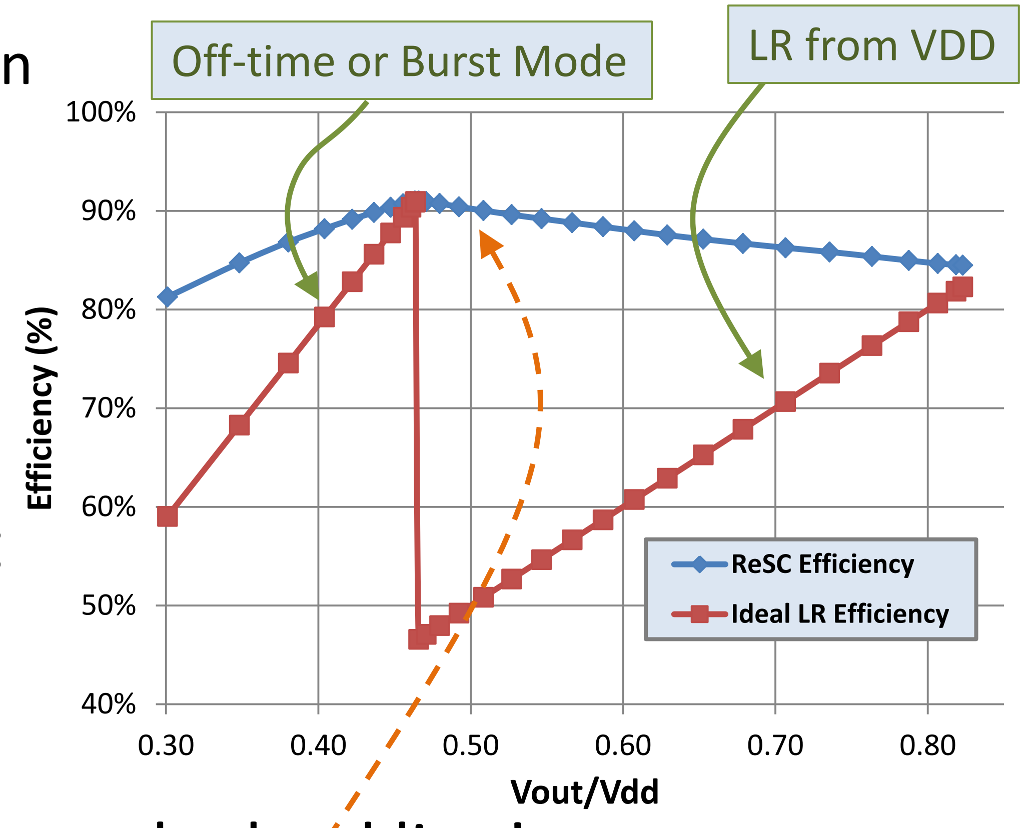


Challenges & Benefits

- Requires hard switching on one transition
  - Possible diode conduction
  - Need fast control

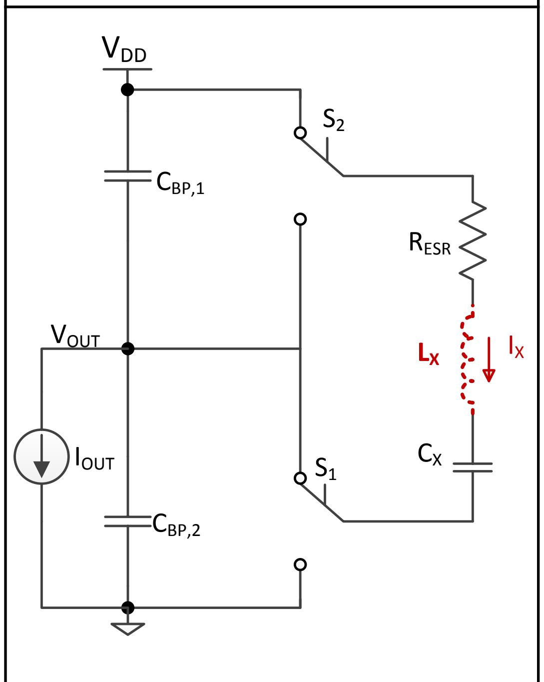
Advantages:

- Potential for high efficiency above/below nominal operating point
- Feedback control & regulation
- Can be used to compensate the load line!



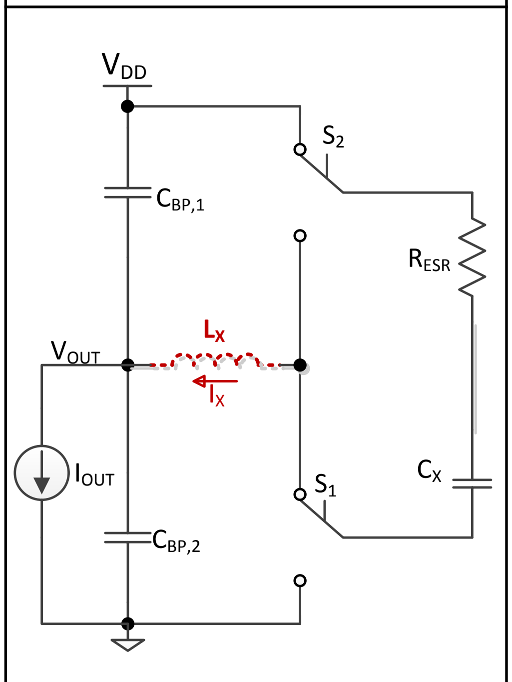
Other ReSC Topologies: Direct vs Indirect

2:1 ReSC
(Indirect Topology)



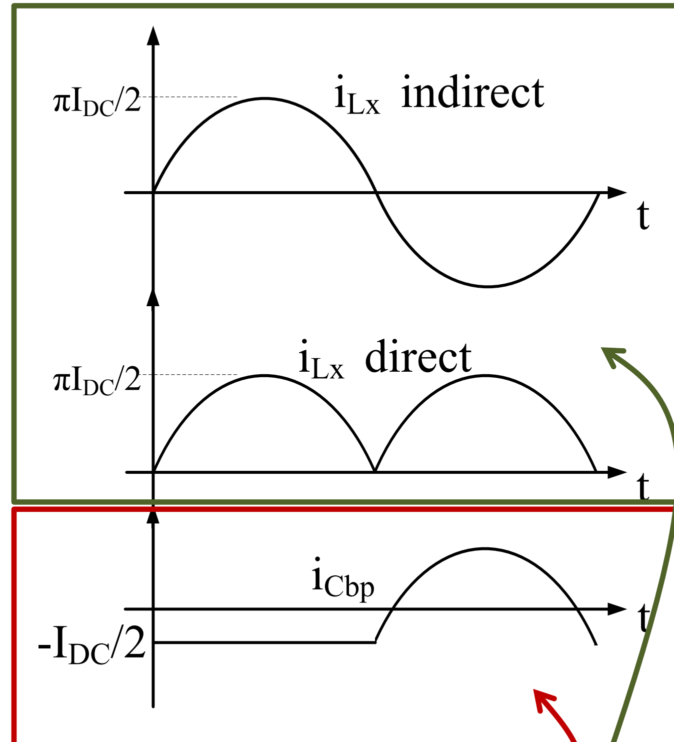
Identical to 2:1 SC but with resonant flying impedance

2:1 ReSC
(Direct Topology)



Similar to 3-level buck converter*; but operates in resonant mode

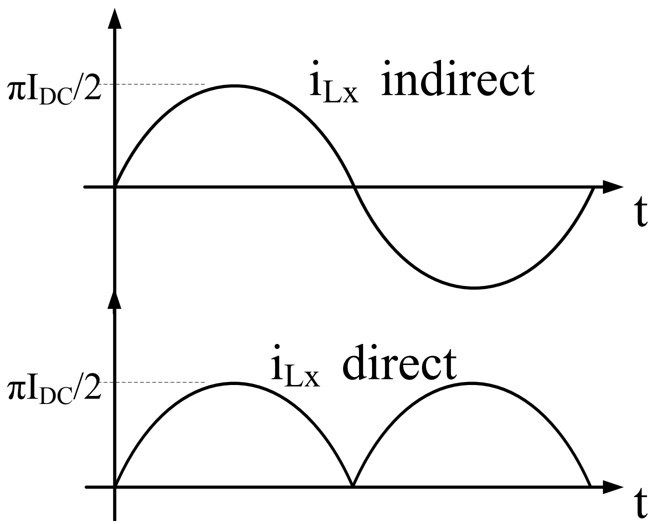
*G.V. Pique, PESC '08



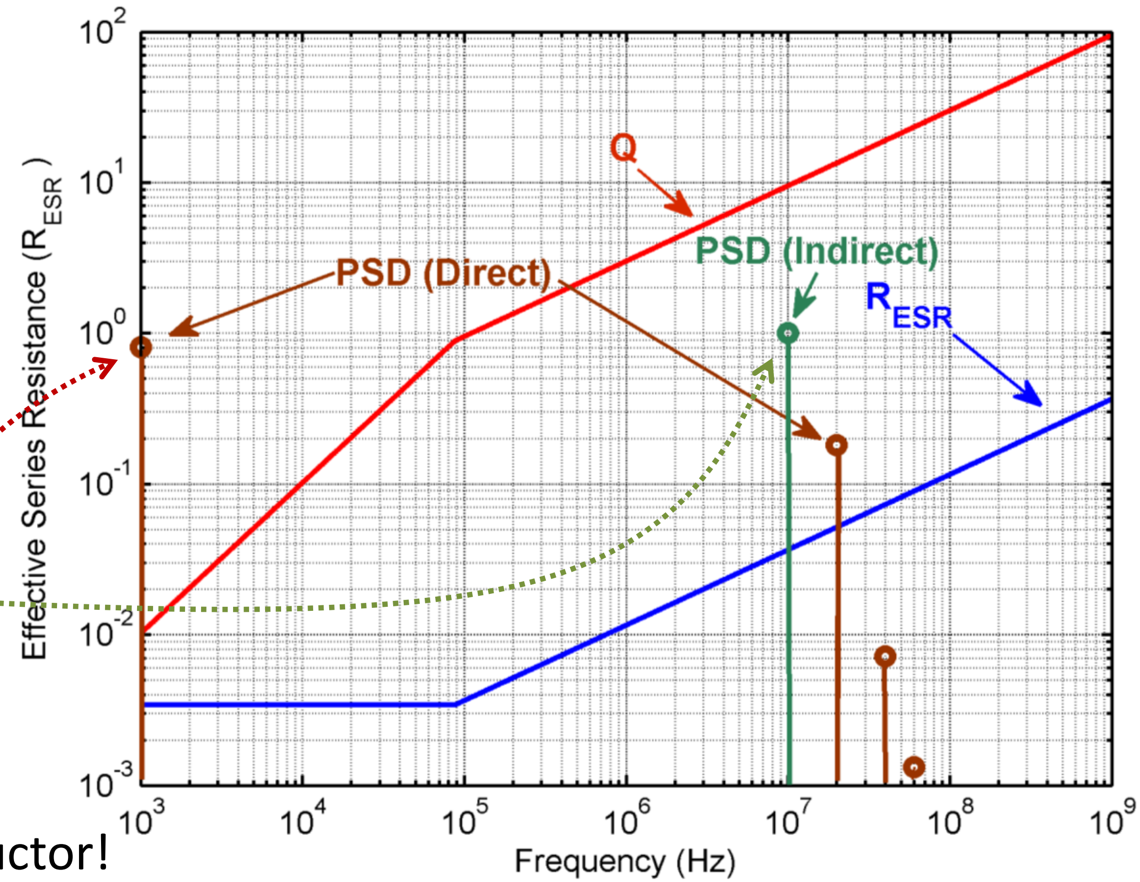
I/O perspective: Identical Operation

Only major difference is current waveform in inductor

Direct/Indirect Comparison



Typical Inductor Characteristics
(Air-Core Solenoid 5.5nH)



Indirect Topology

- ~100% power at f_0

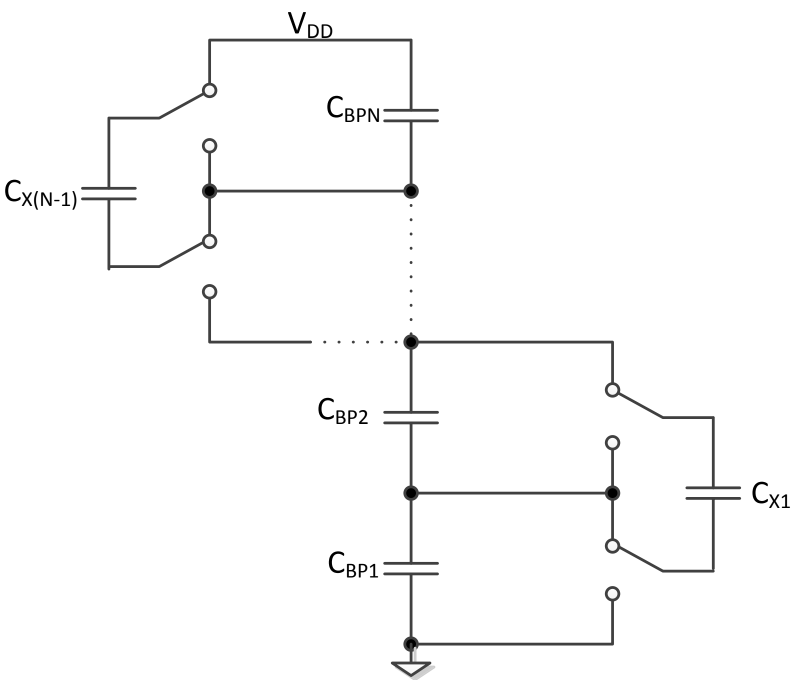
Direct Toplogy

- ~80% of power at DC

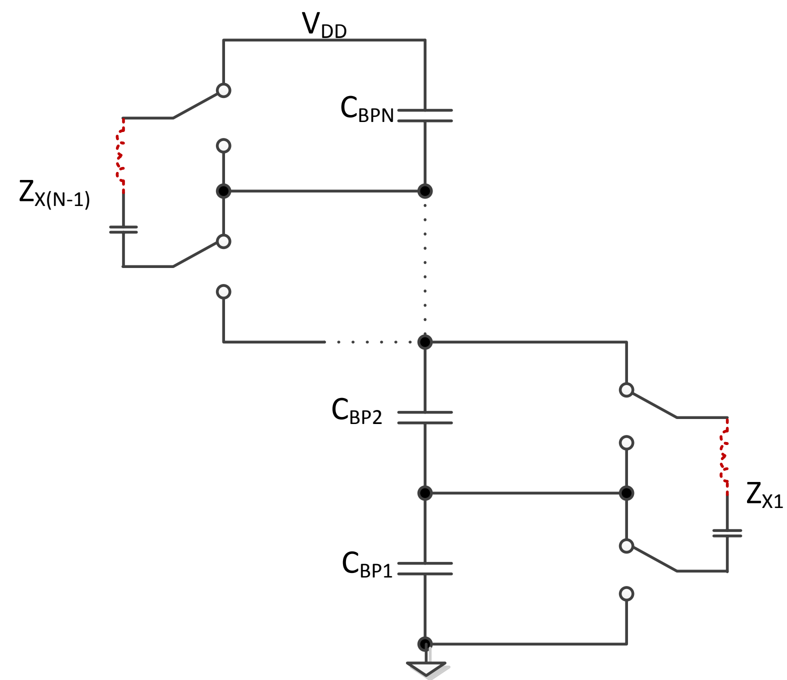
→ Lower conduction loss in inductor!
(ballpark → ~ 3-4x lower)

Other Topologies (Higher Conversion Ratios): Ladder Architecture

N:1 SC Ladder Converter



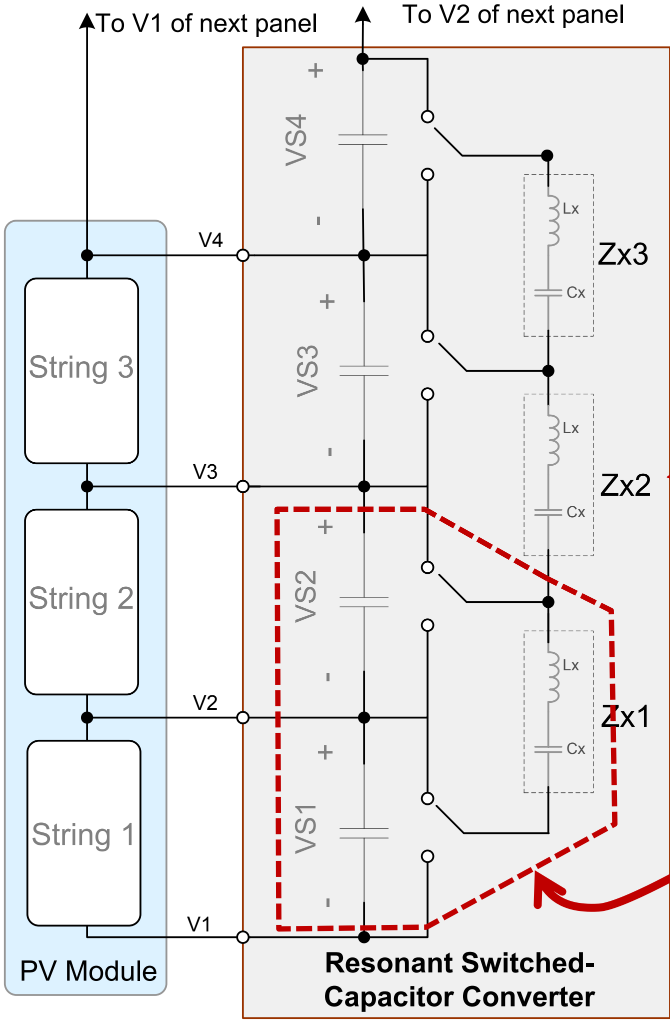
N:1 ReSC Ladder Converter



Requires N-1 magnetic components

Simplest Abstraction: Resonate each flying capacitor in the circuit

Example: Photovoltaic Application

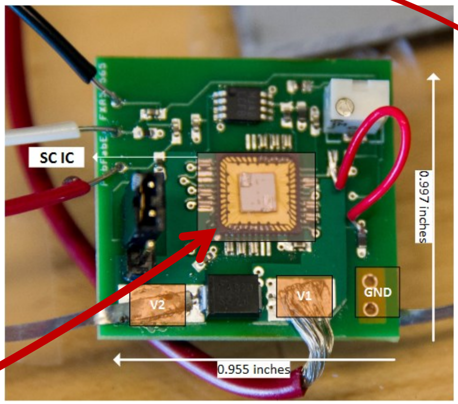


Example 2:

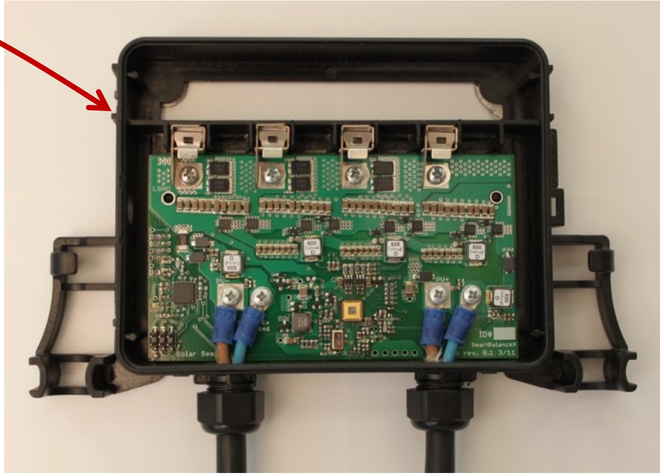
- **IC-Based conv.**
- **4-6 cell strings**
- **< 1 cm²**
- **< 2mm height**
- η_{EFF}>95-98%

Example 1:

- **Many Modules in Series**
- **'Submodule Converter' (~10 V each; stack up to 500V)**
- η_{EFF}>99%
- insertion loss < 0.1 %



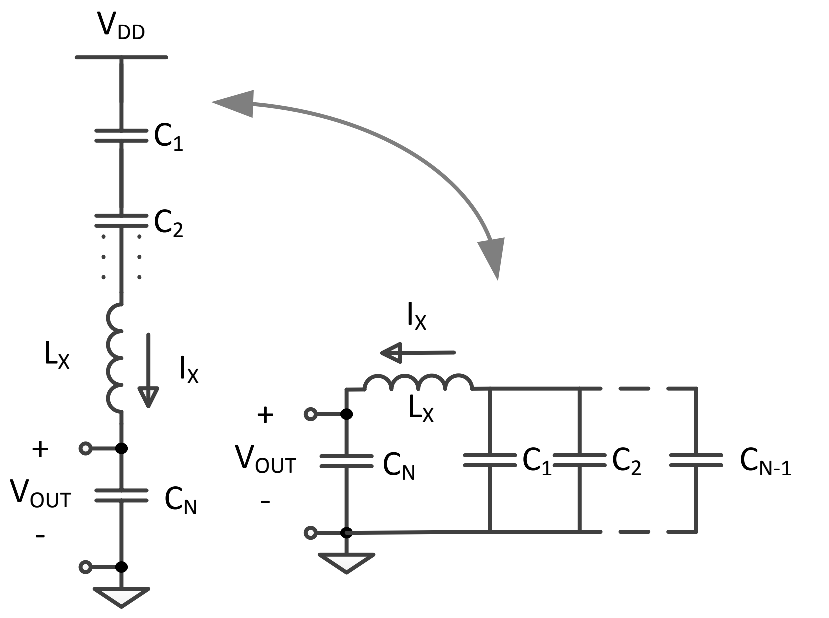
Sangwan et al, ECCE '14



Stauth et al, ISSCC '12, TPEL '13

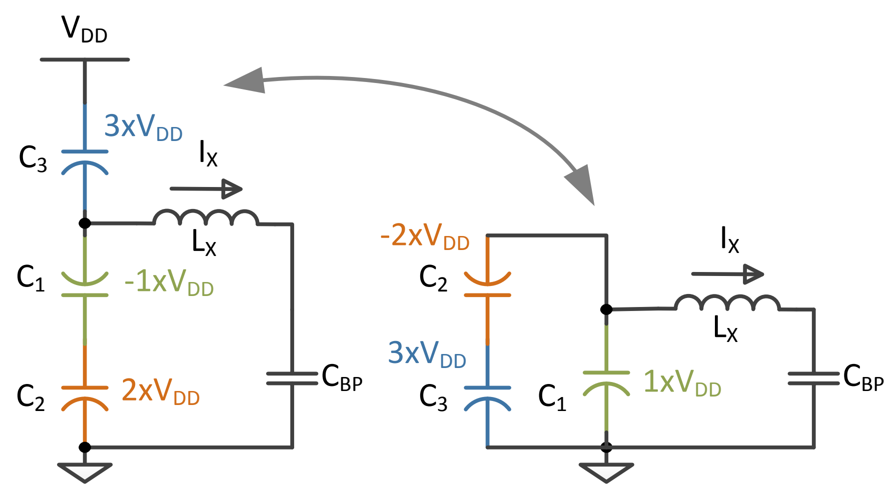
Other Topologies: e.g. Series-Parallel, Dickson

N:1 Series-Parallel ReSC



Devices rated for ~ full stack voltage
Different resonant frequency, each phase

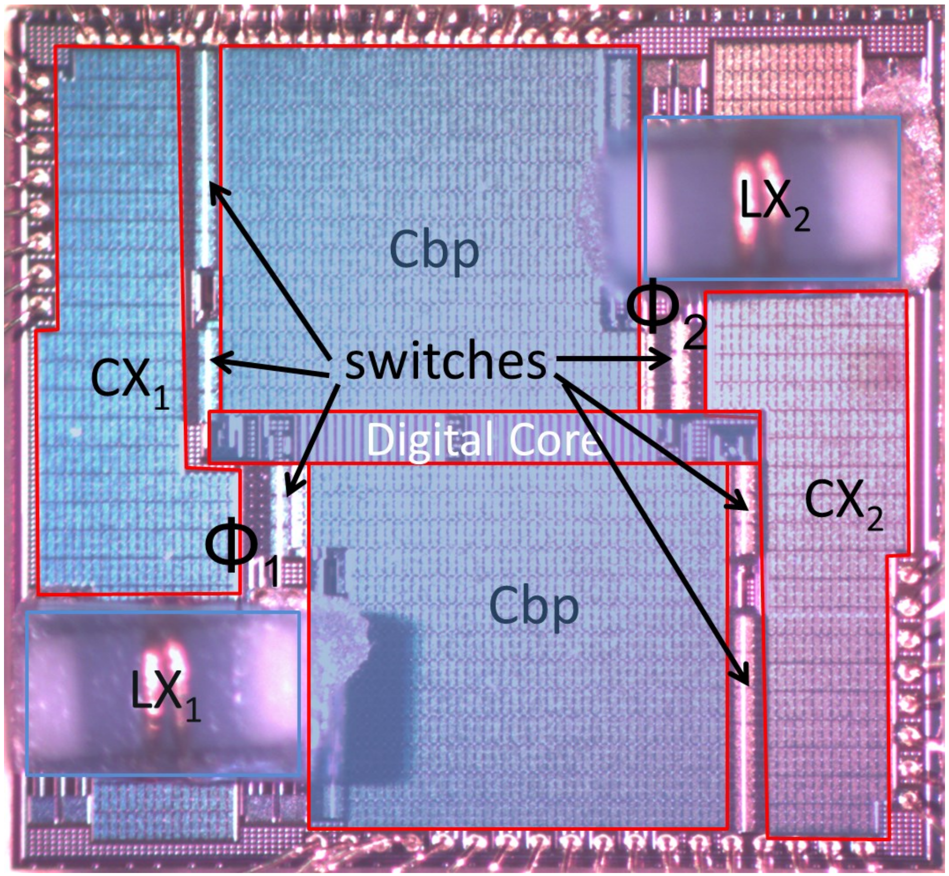
4:1 Dickson ReSC*



Efficient utilization of power devices
Some charge sharing on phase transitions*

*Lei, Pilawa, and May: COMPEL 2013

High-Density Power Delivery: 1st Gen mm-Scale Prototype

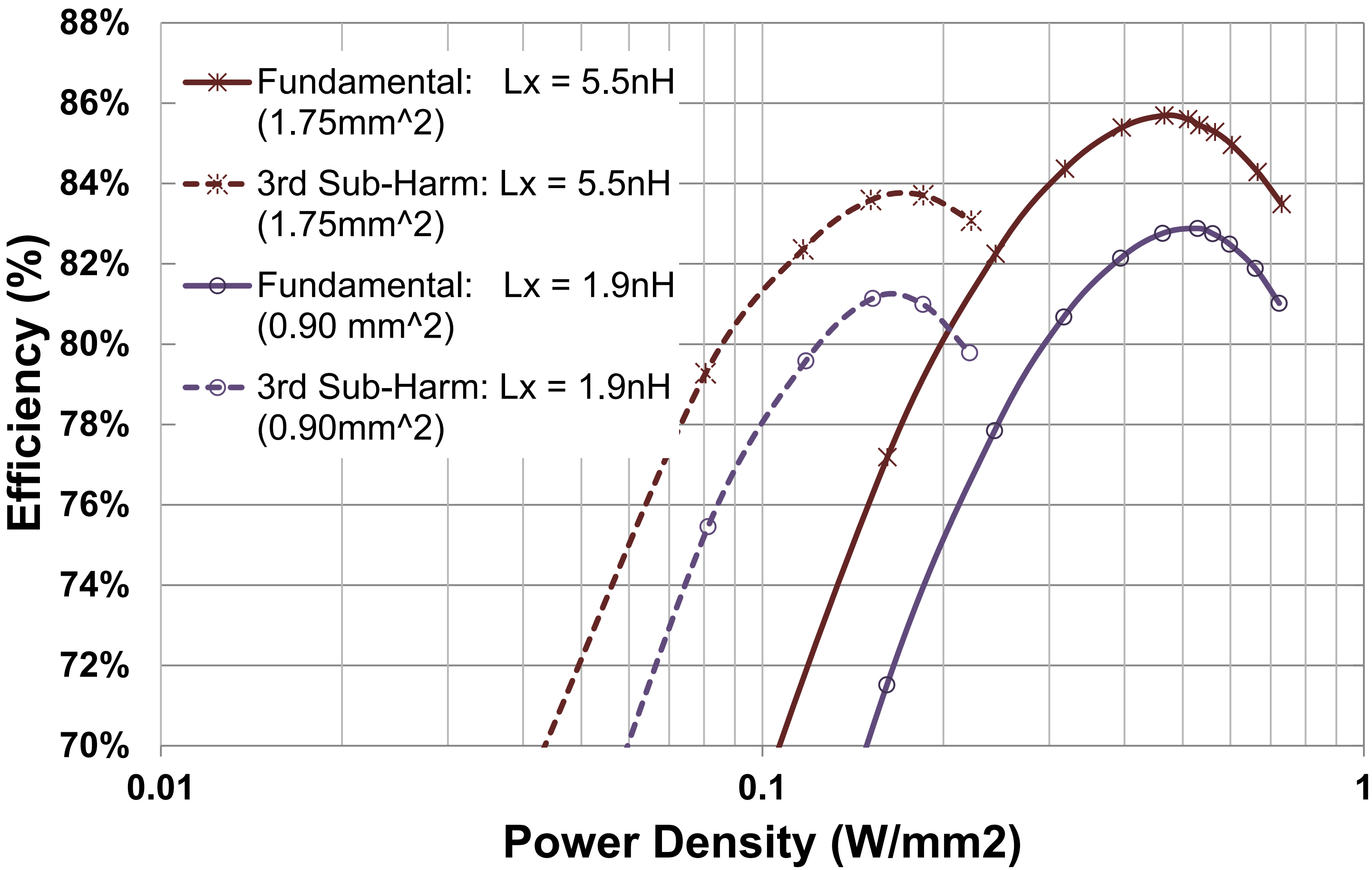


Die-attached air-core solenoid inductors
(gold stud, solder reflow process)

Technology	0.18 µm CMOS
Topology	2-phase ReSC
Conv Ratio	2:1
Vin	~4.5-6 V
Vout	~2-3 V
Frequency	~35 MHz
Cx	9 nF/phase
Cbp	11 nF x 2
Capacitor	MIM: 6.6 fF/um^2

Dynamic Off-time Modulation (DOTM or Burst Mode) for light load & regulation

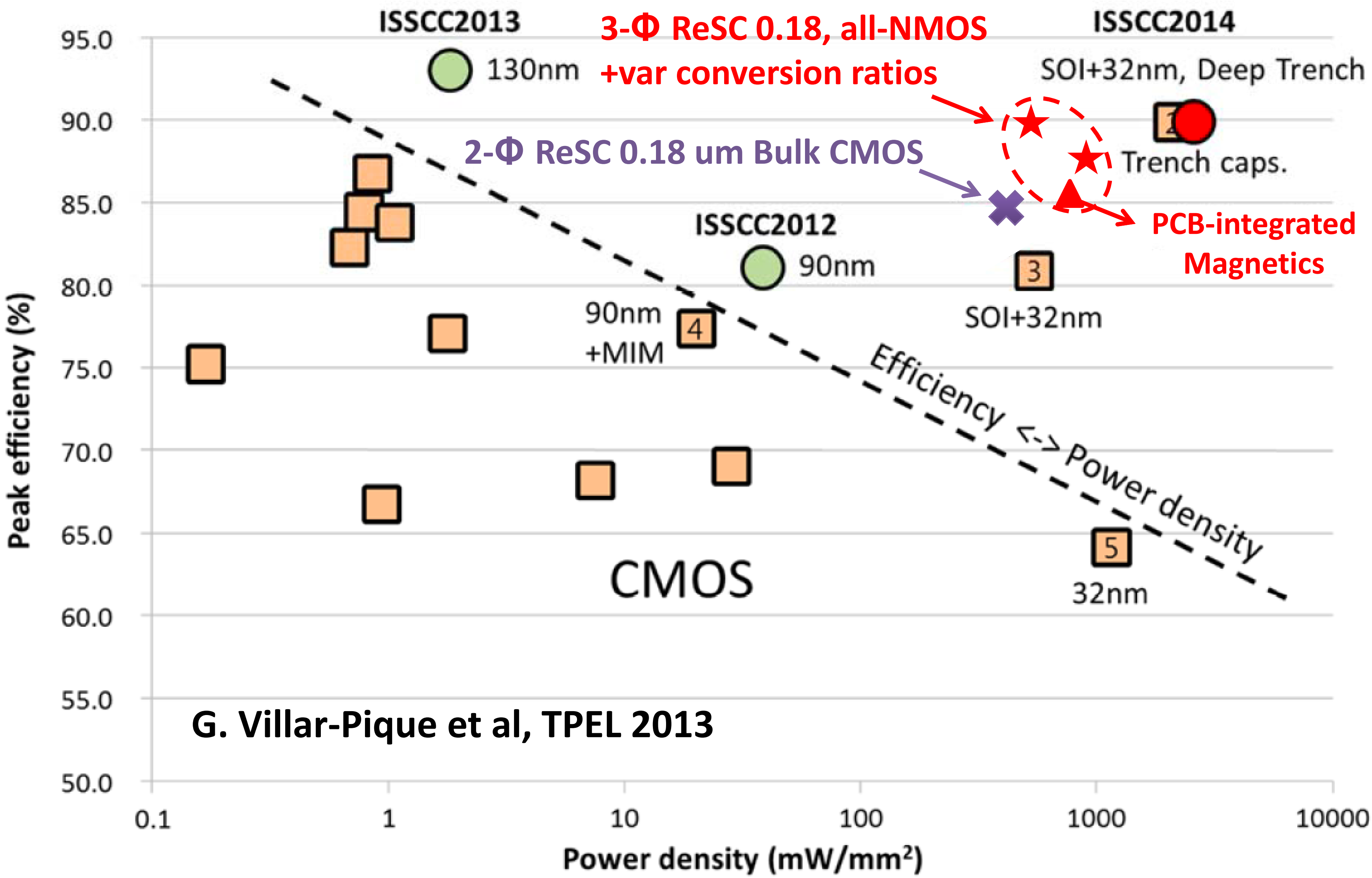
Efficiency Measurements



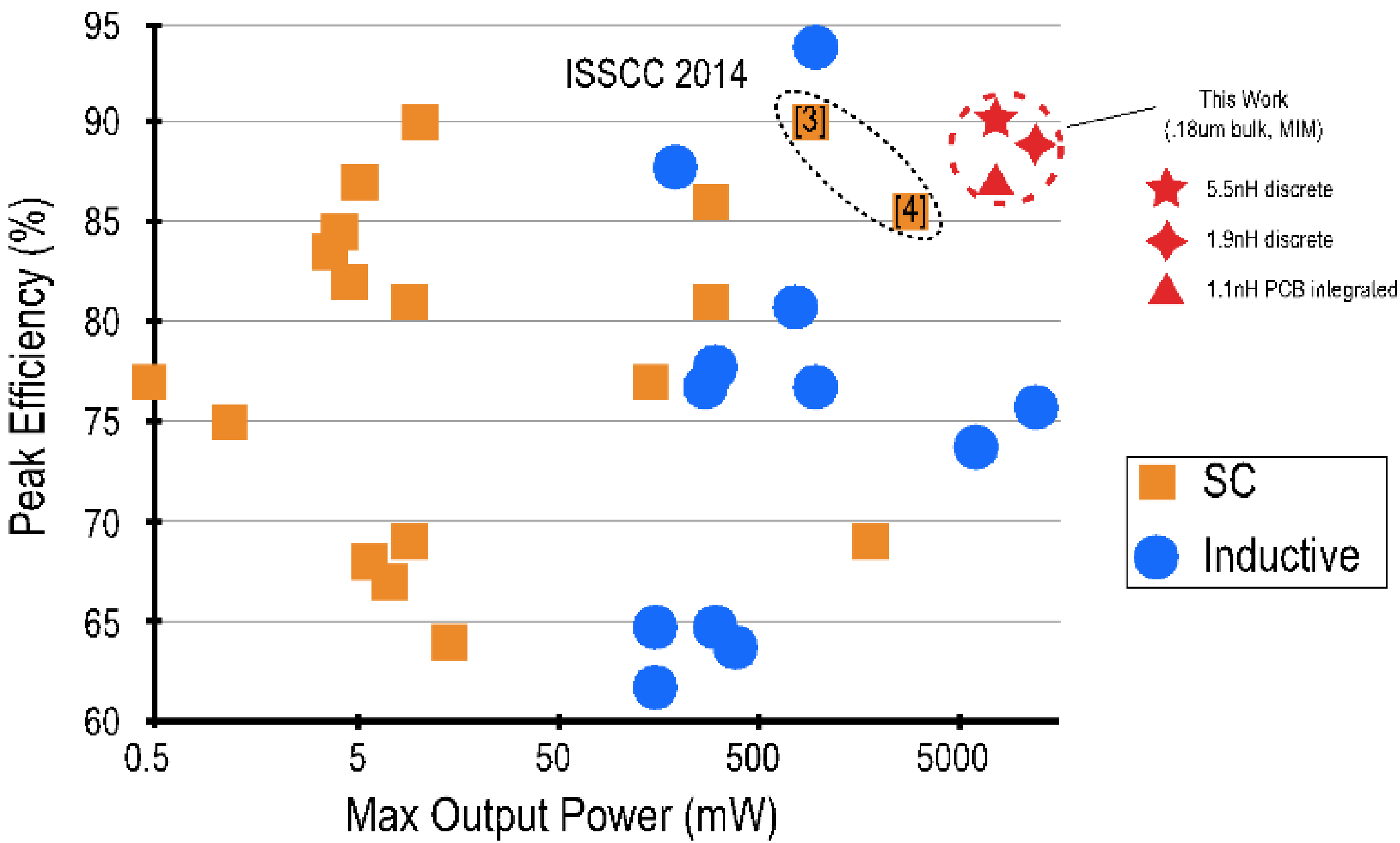
Efficiency of 85.0 % @ 0.60 W/mm^2

Comparison to Prior Work

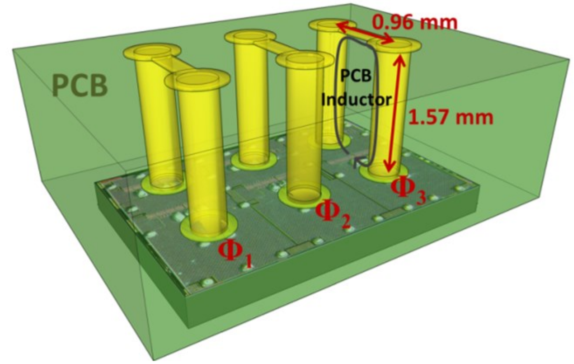
(ISSCC Tech Trends 2014)



Efficiency vs Peak Power

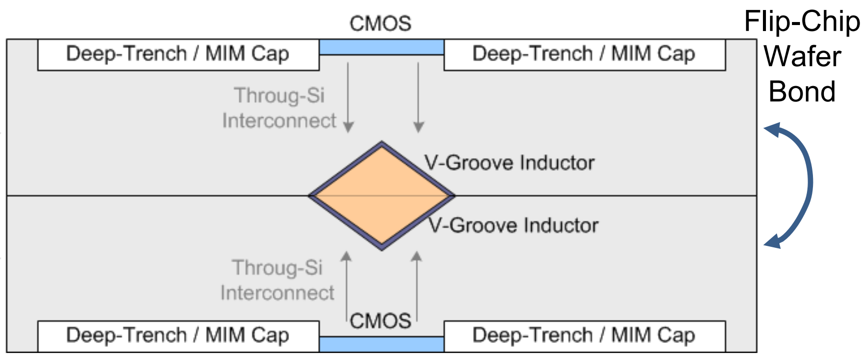


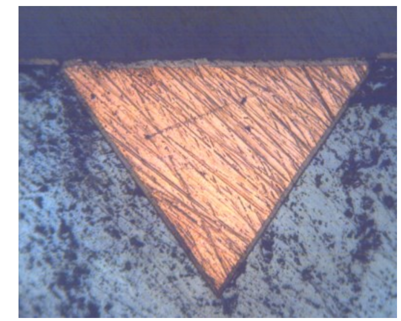
Future Prospects



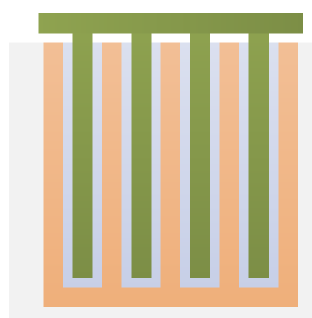
Si-Microfabricated, High-frequency Magnetic Components

e.g. V-groove, Racetrack, Toroidal Inductor (Sullivan et al.)





High-density Cap & Deep-trench processes



Future Goal: Leverage both high-density (trench) caps, and high-frequency microfabricated magnetics

ReSC improves significantly with higher Cap Density and Low ESR Inductors!

References and Acknowledgements

National Science Foundation:
ECCS 1309905
ECCS 1407725

THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

Graduate Students:

Kapil Kesarwani Chris Schaef

Thanks:
Charlie Sullivan

[1] **Stauth, Seeman, & Kesarwani,** *IEEE* ***ISSCC*** **(2012).**

[2] **Kesarwani & Stauth,** *IEEE* ***COMPEL***, **(2012)**

[3] **Stauth, Seeman, & Kesarwani,** *IEEE* ***JSSC*** **(2012).**

[4] **Kesarwani, Schaef, Sullivan, & Stauth**, *IEEE* ***APEC*** **(2013).**

[5] **Stauth, Seeman, & Kesarwani,** *IEEE* ***TPEL*** **(2013).**

[6] **Kesarwani, Sangwan, & Stauth,** *IEEE* ***COMPEL***. 1–7 **(2013).**

[7] **Kesarwani, Sangwan, & Stauth**, *IEEE* ***ISSCC*** 86–88 **(2014).**

[8] **Sangwan, Kesarwani, & Stauth**, *IEEE* ***ECCE*** **(2014)**

[9] **Schaef & Stauth**, *IEEE* ***JESTPE*** **(2014).**